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Design of Parallel Adder/Subtractor using a Novel Reversible Logic Gate

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Abstract: Reversibility plays an important role when energy efficient computations are considered Parity preserving property can be used for this. Reversible logic is a new emerging technology with many promising applications in optical information processing, low power (Complementary Metal Oxide Semiconductor) CMOS design, (De Oxy Ribonucleic Acid) DNA computing, etc. In industrial automation, comparators play an important role in segregating faulty patterns from good ones. In previous works, these comparators have been implemented with more number of reversible gates and computational complexity. All these comparators use propagation technique to compare the data. This will reduce the efficiency of the comparators. To overcome the problem a new 5*5 parity preserving reversible gate is proposed in this paper, named as P2RG. The most significant aspect of this work is that it can work both as a full adder and a full subtractor by using one P2RG and Fredkin gate only. According to the control logic input the proposed design can works as an adder or a subtractor.

Keywords: (De Oxy Ribonucleic Acid) DNA, (Complementary Metal Oxide Semiconductor) CMOS design, P2RG.

I. INTRODUCTION

Reversible circuits are composed of reversible gates. In this circuits there is no information loss. Reversible circuits can produce unique output from each input and vice versa, hence, there is a one-to-one correspondence between input and output vectors (Thapliyal and Srinivas, 2006). So a reversible logic gate has an equal number of inputs and outputs (k ×k) (Babu and Chowdhury, 2005).

In ideal conditions, a reversible circuit has zero internal power dissipation because, it does not lose information. Under R. Landauer's research in the early 1960s, the amount of energy dissipated for every irreversible bit operation is given by KTLn2 joules, where K = 1.3806505 × 10!23 J/K is the Boltzmann's constant and T is the absolute temperature at which operation is performed. But in 1973, Bennett showed that KTLn2 joules of energy can be saved from a system as long as the system permits the regeneration of the inputs from produced outputs (Haghparast et al., 2009; Haghparast and Navi, 2008a; Thapliyal and Gupta, 2006).

A reversible gate with n-inputs and n-outputs is called a n × n reversible gate (Sastry et al., 2006). In a n × n reversible function, there are 2n input rows and 2n output rows in its truth table. In fact the output rows are a permutation of the input rows in the truth table (Kerntopf, 2002; Hung et al., 2006). Direct fan-outs from the reversible gate and feedbacks from a gate output directly to its inputs are not allowed (Sastry et al., 2006). Classical logic gates are called irreversible since they cannot uniquely reconstruct the input vector states from the output vector states. Synthesis and designing of a reversible gate is different from traditional logic gates (Haghparast and Sheikh, 2011). Therefore, constructing a fault tolerant reversible circuit is much more difficult than a conventional logic circuit (Parhami, 2006). In this paper, we propose a fault detection method based on parity preserving reversible logic gate.

Present irreversible technologies dissipate a lot of heat in terms of bit loss which reduces life of the circuit. All logical operations in today's classical computers are irreversible.

It means extraction of input from the respective output is not possible. On the other hand, reversible computation has a salient feature of unique one to one mapping between inputs and outputs which reduces the major problem of power dissipation with no information loss.

A Reversible logic is characterized by:
1. Equal number of inputs and outputs.
2. There exists one to one mapping between the respective inputs and outputs.
3. Loops and fan out are not allowed.

In classical computers, only NOT gate performs reversible operation since it has an equal number of inputs and outputs with their unique one to one mapping. Some reversible gates have already been proposed in literature like the controlled-not (CNOT) (proposed by Feynman) [3], Toffoli and Fredkin gates [4], IG Gate[5] and MIG gate [6]. Reversible gates have various application in the designing of adders, subtractors, multipliers[7], [8] etc, same like classical computers. The main focus of this paper is to design a circuit that can work as adder as well as subtratctor simultaneously with minimum numbers of garbage outputs, constant inputs and area.

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II. DESIGN CONSTRAINTS AND DEFINITIONS

Minimizing the number of Ancillary (constant) Inputs: An extra, auxiliary bit or fixed qubit state that is added to the primary inputs in order to achieve the specific functionality but they need to be minimized for minimizing auxiliary storage.

Minimizing the number of Garbage Outputs: Outputs that are not used further, needed only to make the function reversible (which results to minimize area and power).

Minimizing the Gate Count: Number of gates that are used to realize the system is gate count [9].

Fault Tolerance: Any physical device while performing classical or quantum computation is subjected to error either due to noise in the environment or fault in the device. It can be detected by fault tolerant computing. Although reversibility is able to recover bit loss, but it is unable to detect bit errors in the circuit [10]. Recent digital circuit designing is now focusing on the fault tolerant reversible circuits.

Parity Preservation: It can be used for the fault tolerance computation. Faults in the circuit can be detected by comparing the parity of inputs and outputs. The idea of the parity preserving property in the design reversible logic circuits was given by Parhami [11].
It is known that reversible gates have an equal number of inputs and outputs.
$A \oplus B \oplus C \oplus D = P \oplus Q \oplus R \oplus S$
Where A, B, C and D are gate inputs and P, Q, R and S are gate outputs.

III. LITERATURE SURVEY

Reversible logic gates:
NOT gate: NOT gate is a 1×1 gate represented as shown in Fig.1. Since it is a 1×1gate, its quantum cost is zero (Thapliyal and Ranganathan, 2009; Rangaraju et al., 2010).

Feynman Gate (FG): Among the existing 2×2 reversible gates, Feynman gate which is shown in Fig. 2 is the most important gate. It can be represented as Iv = (A, B) Ov= (P = A, Q = A⊕B), where, Iv and Ov are input and output vectors. Since it is a 2×2 gate, it has a quantum cost of 1 Thapliyal and Ranganathan (2009) and Saiful (2010).

Feynman double Gate (F2G): Feynman double gate as a 3×3 reversible gate is shown in Fig. 3. It can be showed as: Iv = (A, B, C) , Ov = (P = A, Q = A⊕B, R = A⊕C) where, Iv and Ov are input and output vectors respectively.
F2G gate is a Feynman gate with one more input and one more output which the control input 'A' defines a second controlled NOT operation (Haghparast and Navi, 2008b). It has the quantum cost of 2.

Toffoli Gate (TG): Toffoli gate is a 3×3 two-through reversible gate as shown in Fig. 4. It means that two of its outputs are same as the inputs. This gate can be represented as:
Iv = (A, B, C) , Ov = (P = A, Q = B, R = AB⊕C)
where, Iv and Ov are input and output vectors respectively.
Toffoli gate is one of the most popular reversible gates and it has quantum cost of 5 (Thapliyal and Ranganathan, 2009; Chung and Wang, 2007).

Peres Gate (PG): Peres gate also known as New Toffoli Gate (NTG) is a 3×3 reversible logic gate. It can be described as:
Iv = (A, B, C) , Ov = (P = A, Q = A ⊕ B, R = AB⊕C)
where, Iv and Ov are input and output vectors respectively.

Fredkin Gate (FRG): Fig.6 shows 3*3 Fredkin gate (FRG). It has A, B and input vector and output vector as P = A,Q= A'B ⊕ AC and R = A'C ⊕ AB.
If control input A = '0' then inputs B and C are showed clearly in outputs, else if A = '1' then inputs B and C are swapped and showed in outputs. It has quantum cost of 5 (Haghparast and Sheikh, 2011; Saiful, 2010).

New gate (NG): Another one of the interesting gate is New gate which is represented in Fig. 7. The advantage of the New gate is that, this gate can produce all the basic gates. It has the quantum cost of 7 (Hasan et al., 2003; Haghparast and Navi, 2007).

Modified IG Gate (MIG): Fig.8 shows 4*4 Modified IG [11] gate. It has A, B, C and D input vector and output vector as P = A, Q = A ⊕ B, R = AB ⊕ C and S = AB' ⊕ D.

Fig. 1: NOT gate

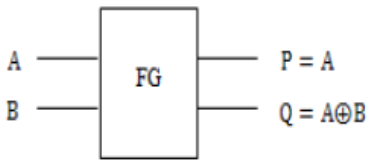

Fig. 2: Feynman gate

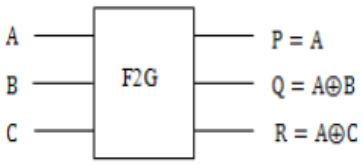

Fig. 3: Feynman double gate

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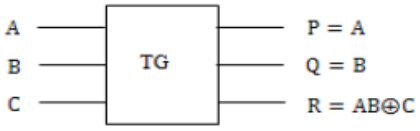


Fig. 4: Toffoli gate

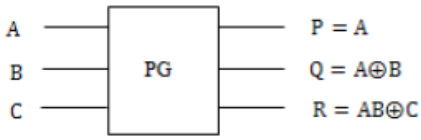


Fig. 5: Peres gate

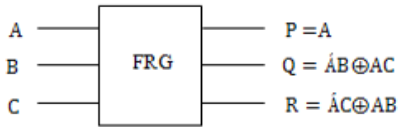


Fig. 6: Fredkin gate

Fig. 7: New gate

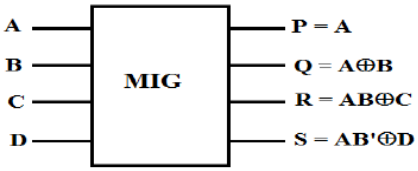
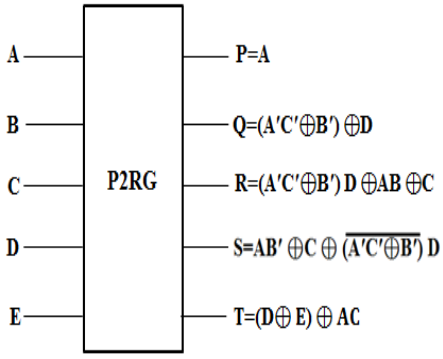


Fig.8 Modified IG Gate (MIG)

IV. PROPOSED DESIGN

A new 5*5 parity preserving reversible gate, P2RG is introduced in Fig.9 (a).

• This gate is one through which means one of its inputs is also an output.
• It is shown in Fig.9 (b) that Proposed gate is universal since it is able to perform NOR operation.



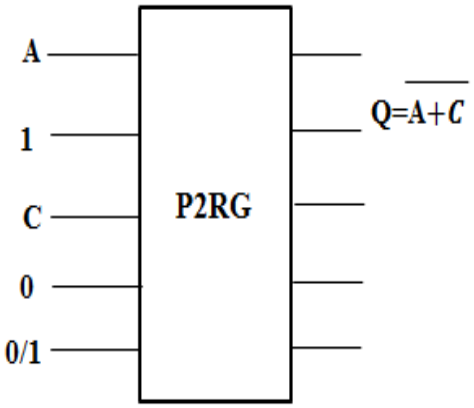


Fig. 9: (a) 5*5 parity preserving reversible gate (P2RG) (b) P2RG as universal gate

When input B= 1 and D= 0 then output Q performs NOR operation i.e. (A+C)'. As it is known that NAND and NOR gates are universal gates so it can be concluded that it can be exploited to realize any arbitrary Boolean function.

Truth table of this gate is shown in Table 1, where A, B, C, D and E are the inputs and P, Q, R, S and T are the outputs. It can be seen from the table that all the input and output vectors are uniquely related. The parity preserving property is promptly verified from the table by comparing the parity of the input to the parity of the output.

TABLE I: Truth Table of P2RG Gate

A	B	C	D	E		P	Q	R	S	T
0	0	0	0	0		0	0	0	0	0
0	0	0	0	1		0	0	0	0	1
0	0	0	1	0		0	1	0	1	1
0	0	0	1	1		0	1	0	1	0
0	0	1	0	0		0	1	1	1	0
0	0	1	0	1		0	1	1	1	1
0	0	1	1	0		0	0	0	1	1
0	0	1	1	1		0	0	0	1	0
0	1	0	0	0		0	1	0	0	0
0	1	0	0	1		0	1	0	0	1
0	1	0	1	0		0	0	1	0	1
0	1	0	1	1		0	0	1	0	0
0	1	1	0	0		0	0	1	1	0
0	1	1	0	1		0	0	1	1	1
0	1	1	1	0		0	1	1	0	1
0	1	1	1	1		0	1	1	0	0
1	0	0	0	0		1	1	0	1	0
1	0	0	0	1		1	1	0	1	1
1	0	0	1	0		1	0	1	1	1
1	0	0	1	1		1	0	1	1	0
1	0	1	0	0		1	1	1	0	1
1	0	1	0	1		1	1	1	0	0
1	0	1	1	0		1	0	0	0	0
1	0	1	1	1		1	0	0	0	1
1	1	0	0	0		1	0	1	0	0
1	1	0	0	1		1	0	1	0	1
1	1	0	1	0		1	1	1	1	1
1	1	0	1	1		1	1	1	1	0
1	1	1	0	0		1	0	0	1	1
1	1	1	0	1		1	0	0	1	0
1	1	1	1	0		1	1	0	0	0
1	1	1	1	1		1	1	0	0	1

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A. Parity Preserving Half Adder/Subtract or

The parity preserving half adder/subtractor is realized using one P2RG gate and one Fredkin gate as shown in Fig.10. Half adder and subtractor are the basic building block to design full adder and subtractor. We need two input i.e. A and B to design a half adder/subtractor. No previous carry or borrow is needed in this. So, this design has two inputs A and B and a control line Ctrl which will control mode of operation, i.e. when Ctrl is at logic 0, the circuit will act as half adder and when ctrl is at logic 1, the circuit will act a s half subtractor. It will give three constant inputs and four garbage bits g1 to g4. Boolean expressions to realize the functionality of half adder and half subtractor are given below:

Sum/Difference = A ⊕ B
Carry = AB
Borrow = A'B

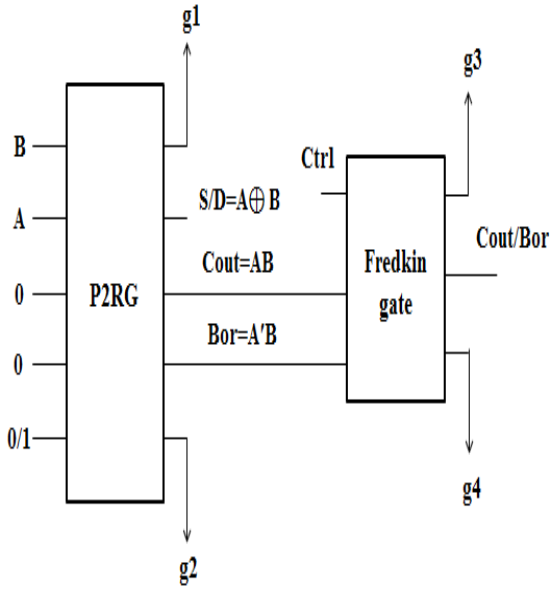

Fig. 10: Parity Preserving Half Adder/Subtractor using P2RG gate

B. Parity Preserving Full Adder/Subtractor

Many adder designs using reversible gates by several authors have been studied. The proposed design will work as adder as well as subtractor on a single unit.

The parity preserving full adder/subtractor is realized using one P2RG gate and one Fredkin gate. In Fig.11, the circuit has three inputs A, B, Cin and a control line Ctrl which will control mode of operation. If Ctrl= 0, it will work as a full adder else it would function as a full subtractor. It has 2 constant inputs, C is set to 0 and E can be set to either 0 or 1. The basic Boolean expressions for sum/difference, carry and borrow are given below for full adder and subtractor:

(Sum/Difference = (A ⊕ B ⊕ Cin))

(Carry = ((A ⊕ B).Cin) ⊕ AB))

(Borrow = ((A)'.B) ⊕ (((A ⊕ B)').Cin))

Proposed circuit is optimized in terms of number of constant inputs and garbage outputs. Fig.11 shows the implementation of parity preserving full adder/ subtractor in which g1, g2, g3 and g4 are garbage outputs.

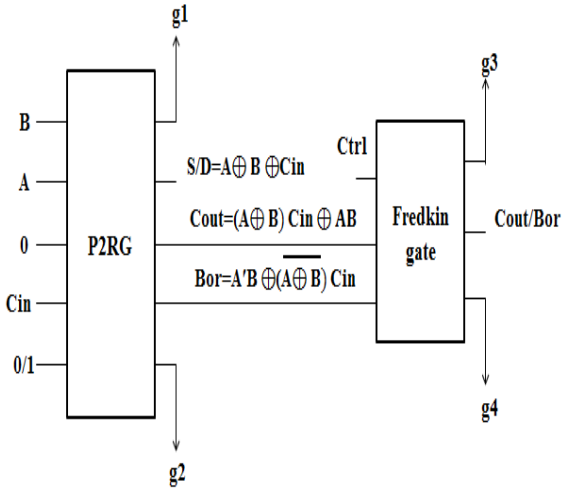

Fig. 11: Parity Preserving Full Adder/Subtractor using P2RG gate

C. Parity Preserving 16 -bit Parallel Adder/Subtractor

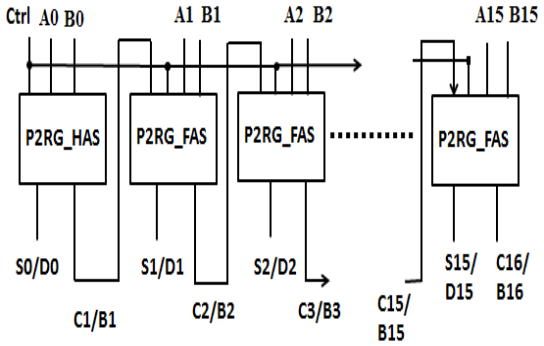

Fig. 12 Parity preserving 16 bit parallel Adder/ Subtractor using P2RG gate

An n-bit parallel adder/subtractor will need a chain of (n-1) full adders/subtractor and one half adder/subtractor. Therefore 16-bit parity preserving parallel adder/subtractor is designed by using one parity preserving half adder/subtractor (P2RG HAS) and fifteen parity preserving full adder/subtractor (P2RG FAS). It has two 16-bit numbers which are A0 to A15 and B0 to B15 as inputs and a control line ctrl which will control the mode of operation. When ctrl line is set at logic 0, the circuit will perform 16-bit addition operation and when ctrl line is set at logic 1, the circuit will perform 16-bit subtraction.

The Carry/Borrow received after addition/ subtraction is represented by C1/B1 to C15/B15.Output carry/borrow of each block, i.e. C1/B1 to C15/B15 will be the third input for the next block. The outputs, Sum/Difference and Carry/Borrow are shown in the Fig.12 as S0/D0 to S15/D15 respectively. Fig.12 shows the parity preserving 16-bit parallel adder/subtractor.

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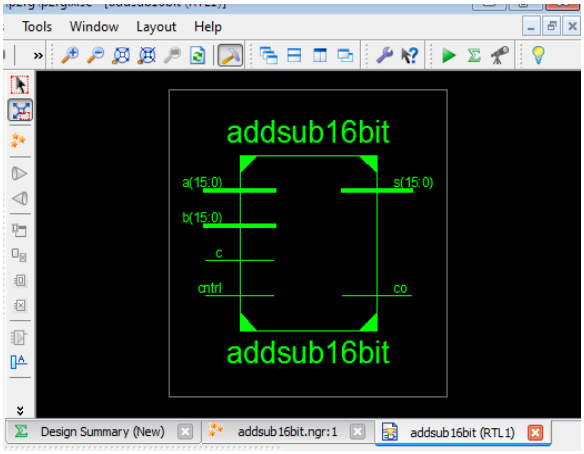
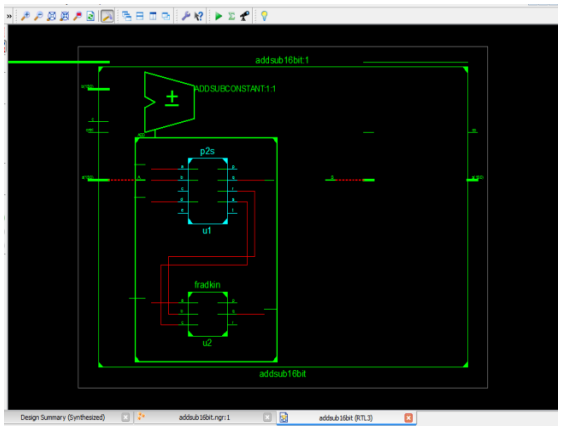
V. RESULTS

The entire architecture is modeled using Verilog. The coding is done on Xilinx ISE12.1 (xc6slx41-1ltqg144) at speed grade of -1. RTL Schematic view, Simulation and Timing report of 16 Bit Parallel Adder/Subtractor are shown in the following figures



(a)



(b)

Fig: 13 (a), (b) RTL Schematic of Proposed 16 bit parallel adder/subtractor

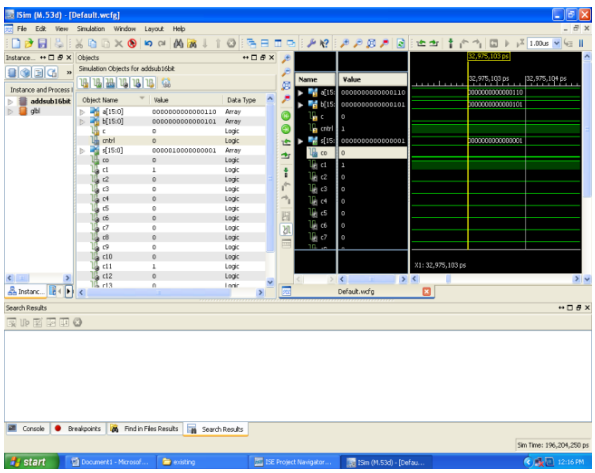


Fig 14. Simulation Result of Proposed 16 bit Adder/ Subtractor when ctrl=1(it acts as a Parallel Subtractor)

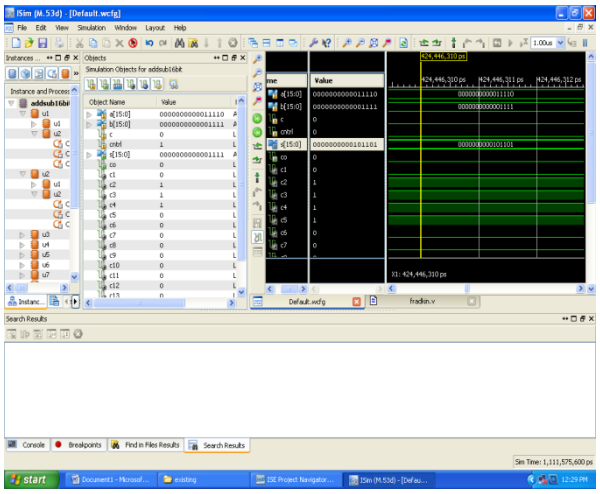


Fig 15. Simulation result of Proposed 16 bit Adder/ Subtractor when ctrl=0 (it acts as Parallel Adder)

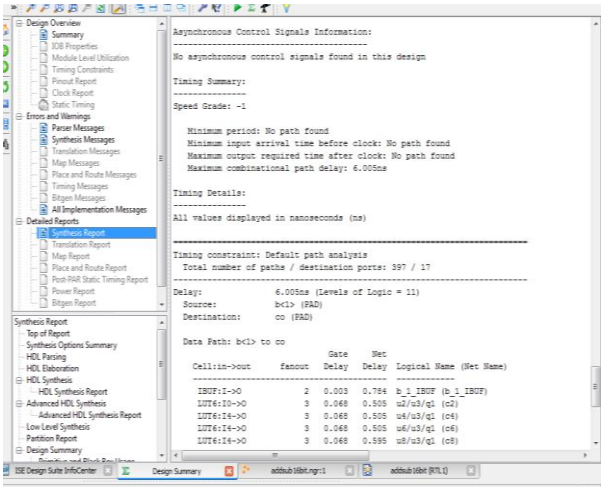


Fig 16. Timing report of Proposed 16 bit Parallel Adder/Subtractor

VI. APPLICATIONS

Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. It is not possible to realize quantum computing without implementation of reversible logic

VII. CONCLUSION

In this study, we proposed a novel Parity Preserving Reversible gate. We also designed Parity Preserving Half-Adder/Subtractor circuit and a Parity Preserving reversible full-Adder/Subtractor circuit using P2RG gate. The proposed design can work as single unit that can acts as adder as well as subtractor depending upon our requirement. The proposed design offers less hardware complexity, less gate count, less garbage bits and constant inputs.

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VIII. FUTURE SCOPE

In this paper we have worked on the Reversible logic gates on combinational circuits in future we can extend these to implement sequential circuits also.

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